REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action of August 29, 2008 (hereinafter "Office Action"). Applicants have amended Claims 12, 16, 18, 20, 21, 23, 27, 28 and 30 as set out above to address issues raised in the Response to Arguments section of the Office Action on pages 2-3. Accordingly, Applicants respectfully submit that the pending claims are patentable for at least the reasons discussed herein.

As a preliminary note, Applicants would like to point out that since rejections from previous Office Actions have been maintained in the present Office Action, in the interest of brevity, Applicants will not repeat the arguments made in Applicants' Previous responses herein. However, Applicants incorporate the relevant arguments made in their previous responses of March 14, 2008 by reference as if set forth in its entirety herein. Accordingly, Applicants will limit their response to addressing the Amendments to Claims 12, 16, 18, 20, 21, 23, 27, 28 and 30 and responding to the Response to Arguments section beginning on page 2 of the Final Action.

The Section 102 Rejections

Claims 12-19 and 30 stand rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,583,362 to Maegawa (hereinafter "Maegawa"). *See* Office Action Action, page 4. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by Maegawa. For example, amended Claim 12 recites:

> A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:
>
> forming a MOS transistor on an integrated circuit substrate including an isolation layer and an active region higher than the isolation layer, **the MOS transistor having a pair of junctions consisting of a vertical source region and a vertical drain region on the isolation layer**, and a plurality of gates on the active region, the plurality of gates being stacked between the vertical source region and the vertical drain region;
>
> **forming a horizontal channel between the vertical source region and vertical drain region, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns, wherein the pair of junctions are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns so that the pair of vertical junctions contact the sides of the at least two spaced apart horizontal channel regions**; and

forming a vertical source electrode electrically connected to the vertical source region and a vertical drain electrode electrically connected to the vertical drain region.

Applicants respectfully submit that at least the highlighted recitations of amended independent Claim 12 are neither disclosed nor suggested by Maegawa for at least the reasons discussed herein.

The Office Action points to Figure 30 of Maegawa as teaching all of the recitations of Claim 12. *See* Office Action, page 4. However, it is clear from Figure 30 of Maegawa that Maegawa discusses plurality of vertically stacked sources and drains each contacting with corresponding vertically stacked channels. In other words, Maegawa discloses a plurality of vertically stacked junctions. In stark contrast, the present application discusses one source region and one drain region that are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns so that one source region and one drain region contact the sides of the at least two spaced apart horizontal channel regions. Nothing in Maegawa discloses or suggests "a pair of junctions consisting of a vertical source region and a vertical drain region that contact the vertically stacked channels" as recited in amended Claim 12. Accordingly, Applicants respectfully submit that Claim 12 and the claims that depend therefrom are patentable over Maegawa for at least the reasons discussed herein.

Amended independent Claim 30 recites:

A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:

forming a horizontal channel between **a vertical source region and a vertical drain region**, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns; and

forming the vertical source region and the vertical drain region in other patterns at one side of the spaced apart patterns, respectively.

Applicants respectfully submit that the highlighted portions of independent Claim 30 are patentable over Maegawa for at least reasons similar to those discussed above with respect ot Claim 12.

The Section 103 Rejections

Claims 20-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Maegawa in further view of United States Patent No. 6,420,758 to Nakajima (hereinafter "Nakajima"). *See* Office Action, page 8. Applicants respectfully submit that many of the

recitations of these claims are neither disclosed nor suggested by Maegawa. For example, amended Claim 23 recites:

> A method of fabricating a transistor comprising:
> forming a trench region on an integrated circuit substrate to define an active region;
> forming a stacked structure including at least one set of first epitaxial patterns and second epitaxial patterns on the active region;
> forming a first insulation pattern on a floor of the trench;
> growing a third epitaxial layer on sidewalls of at least one set of first and second epitaxial patterns;
> forming a second insulation pattern on a surface of the integrated circuit substrate, the second insulation pattern defining a gate opening that exposes at least a portion of the third epitaxial layer;
> removing the third epitaxial layer in the gate opening to expose the set of at least one first and second epitaxial patterns;
> selectively etching the first epitaxial patterns of the set of at least one first and second epitaxial patterns to form a horizontal channel region having a plurality of spaced apart channel layers;
> forming a gate oxide layer on a surface of channel layers;
> forming a gate pattern on the horizontal channel and in gap regions between the channel layers and the gate opening; and
> **forming a vertical source electrode and a vertical drain electrode** penetrating the second insulation pattern to be connected to the third epitaxial layer.

Applicants respectfully submit that at least the highlighted recitations of amended independent Claim 23 are neither disclosed nor suggested by the cited combination for at least the reasons discussed herein.

The Office Action points to Maegawa combined with Nakajima as teaching all the recitations of Claim 23. *See* Office Action, pages 11-12. As discussed above, Maegawa discusses plurality of vertically stacked sources and drains each contacting with corresponding vertically stacked channels. In other words, Maegawa discloses a plurality of vertically stacked junctions. In stark contrast, a single vertical source electrode and a single vertical drain electrode. Nothing in Maegawa discloses or suggests at least these recitations of the claim. Accordingly, Applicants respectfully submit that Claim 23 and the claims that depend therefrom are patentable over Maegawa for at least the reasons discussed herein.

CONCLUSION

Applicants respectfully submit that pending claims are in condition for allowance, which is respectfully requested in due course. Favorable reconsideration of this application is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,

Elizabeth A. Stanek
Registration No. 48,568

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on December 1, 2008.

Candi L. Riggs